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1. Past Programs

Metrology has been a significant factor in the advancement of the semiconductor device industry. Understanding and control of both dimensional characteristics and materials properties have been essential in the development, design, and production of transistors and integrated circuits since their invention. The trend to very large scale integration (VLSI) increases the metrological requirements associated with each of these areas.[1]

The National Bureau of Standards (NBS), as the Nation's research laboratory for measurements and physical standards, has been concerned with measurements for semiconductor materials and devices since about 1960.[2] From the start, this activity has been very selective; research projects have been chosen and carried out on the basis of close interactions with the producing industry, its suppliers, and users in other Federal agencies and in the private sector. Early projects on silicon resistivity and transistor second-breakdown measurements have expanded to become the Semiconductor Technology Program which covers a broad spectrum of research activity on techniques for characterizing electronic materials, including silicon and other semiconductors, insulator films, metal interconnects, process chemicals, and resists; and techniques for measuring pattern dimensions, selected electrical and thermal properties of devices, interconnection and die bond quality, package integrity, and other critical quantities. The primary outputs of this program include improved measurement methods, prototype measuring instruments, interpretive theory, and supporting data. It is important to emphasize that it does not include development of new device designs, new processing or assembly techniques, or new manufacturing equipment, except as these may be ancillary to the primary outputs.

This activity is carried out at the Washington complex of the NBS in the Electron Devices Division which is a part of the Center for Electronics and Electrical Engineering, one of the Bureau's 13 scientific and technical centers. Financial support for the work has come both from direct appropriations and from funds transferred by other Federal agencies, principally the Departments of Defense and Energy and the National Aeronautics and Space Administration. Most of the Bureau's research is conducted in-house; in the present program a significant fraction of the research that was funded by ARPA was carried out by outside contractors during the late 1970s, but major contract activity is not expected to continue into the future.

Among the early projects with the greatest impact on the semiconductor industry are those concerned with the four-probe method for measuring resistivity of silicon slices,[3] test methods for wire bonding,[4-6] and thermal resistance measurements on power transistors.[7] Research on each of these topics was undertaken in response to defined industrial needs as articulated by an industrial standards committee or by a concerned Federal agency.

Identification of priorities for NBS work in this way is particularly important because NBS does not establish specifications, is not a major procuring agency, and has no regulatory authority. The results of the work were implemented in many different ways which are typical of the diverse relationships between the NBS program and the industry.

In the case of the resistivity work, which was undertaken in response to a request from Committee F-1 on Electronics of the American Society for Testing and Materials, results were implemented in three phases. Early interim results, such as geometric correction factors, data on the temperature coefficient of resistivity and specimen preparation techniques, were reported to the Committee and in the literature as they were obtained. In this way, interested parties were able to incorporate the findings in their routine measurement procedures for both materials acceptance and process control before the project was completed. As the work neared completion, the results were incorporated into an ASTM standard[8] which became the referee method for the industry and also into four other related ASTM standards. Finally, several types of sets of silicon slices were certified as to their resistivity as measured in accordance with the ASTM method[8] and issued as standard reference materials (SRMs) by NBS.[9] These SRMs continue to be useful reference standards; although the industry is presently shifting from the four-probe method to a contactless technique[10] for routine resistivity measurements, the newer method requires the use of standards to provide calibration at several values of resistivity.

The wire-bond work was undertaken in response to the needs of a military agency. The initial output was a new method for monitoring the ultrasonic bonding process.[4] Use of this method together with a novel scanning electron microscope examination technique[11] led to greatly increased understanding of the process, to suggestions for improvements in bonding machine design (many of which were incorporated by equipment makers through retrofits or in next-generation machines and thus introduced painlessly into the device manufacturing process), to a sound basis for the nondestructive pull test,[12] and to substantial improvements in productivity and in device and system reliability. In this instance, the results were incorporated first on captive lines operated in several companies on behalf of a major military system; they then diffused through the industry and were eventually embodied in ASTM standards[13,14] and in the bond test methods of the military standards for discrete devices[15] and integrated circuits.[16] The interlaboratory test to evaluate the destructive pull test[14] identified and led to the solution of a variety of problems including a potential deficiency in a widely used automatic pull tester.[17]

The thermal resistance work was an outgrowth of the early work on second breakdown in transistors. The project was carried out in close collaboration with various committees of the Joint Electron Devices Engineering Councils (JEDEC). The work led to identification of a preferred electrical test method and its range of application which was issued as an Electronic Industries Association Recommended Standard[18] and incorporated in a military standard.[19] The results of this work formed the basis for a commercial thermal resistance test instrument and eventually led to a new method for determining the safe operating area of power transistors.[20]

2. Future Directions

Some of the more recent projects in the program relate directly to some of the metrological requirements of VLSI. One critical requirement relates to dimensional metrology of integrated circuit pattern features in the 0.5- to 10-μm range on photomasks[21] and wafers.[22] This work was undertaken following an extensive industry survey[23] which established the need for linewidth measurements in this regime. Procedures have been developed for making linewidth measurements on photomasks, SRMs are being made available to the industry, and ASTM standards are under development. These procedures have also been extended to patterns in very thin oxide layers on silicon; extension to patterns in technologically more interesting layers greater than 0.2 μm thick is underway. In addition, the techniques are being transferred to the industry in a series of training seminars which feature hands-on experience with linewidth measuring systems loaned for the purpose by instrument manufacturers. From time to time, multilaboratory tests are conducted to assess the state of the measurement art in this field.

Microelectronic test structures are device-like elements used to measure selected critical material and process parameters by means of high-speed electrical tests.[24] They are particularly important in connection with design rule verification and in establishing, verifying, and controlling wafer fabrication processes. Work in this area was undertaken following both extensive informal discussions with industry representatives and conduct of a workshop[25] held to provide a more formal channel for discussions on this topic. A wide variety of structures have been investigated including a cross-bridge array for evaluation of pattern generators and step-and-repeat cameras, a production-compatible potentiometric electrical alignment test structure which has been shown to be sensitive to misalignments of 0.1μm, and both serial and random-access structures to test for random fault distributions. In addition, test structures for use in measuring material properties with conventional automatic wafer probers and dc instrumentation are also being studied. Among the more advanced of these are the four-terminal enhancement-mode MOSFET, with which dopant profiles can be measured,[26] and the gated diode test structure with integral transistor switch and source-follower MOSFET electrometer, which facilitates the measurement of small leakage currents and the determination of generation lifetime and surface recombination velocity.[27]

Both the dimensional metrology and microelectronic test structure efforts are being extended in connection with the Defense Department's program to develop very high speed integrated circuits (VHSIC). In addition, the Commerce Department plans to undertake an initiative on Basic Measurements for Very Large Scale Integration (VLSI) beginning late in 1980. This initiative is intended to provide the same types of technical outputs as the ongoing Semiconductor Technology Program, extended to accommodate the denser circuits, larger chips, and new processing techniques associated with VLSI. The augmented program will address the six critical areas listed in table 1. Although rather detailed preliminary plans have been developed, it is essential to emphasize that considerable flexibility is required in order to enable the program to respond to industry requirements as they develop. It is also important to realize that, as has been done in the NBS Semiconductor Technology

Table 1 – VLSI Program Elements

- Silicon characterization
- Interface characterization
- Process control metrology
- Microelectronic test structures
- Package evaluation
- Testing

Program heretofore, many of these activities involve much more than simply finding a way to make a measurement. Fundamental work to develop a clear understanding of the basis for the measurement and its range of utility is often required as well. Key issues within each area are expected to include the following:

Silicon characterization: methods for profiling the distribution of dopant impurities, especially in shallow, low-dose ion implantations; methods for characterizing nondopant or deep-level impurities and resolution of differences between results obtained by various methods; identification of appropriate parameters to be specified for substrate wafers; and techniques for characterizing wafer surface distortion.

Interface characterization: methods for measuring neutral trap densities and distributions near silicon-silicon dioxide interfaces; techniques for characterizing the structural and electrical properties of this and other device interfaces; techniques for evaluating multilayer metal interconnect systems; and methods for measuring contact resistance at the interconnect-semiconductor interface.

Process control metrology: methods for measuring linewidth and edge quality in small features with large aspect ratio (height to width); measures for sensitometry and other attributes of resists; and metrology associated with control of processes such as plasma etching, ion implantation, laser annealing, and ion milling.

Microelectronic test structures: scaling to VLSI dimensions of test structures for measuring material characteristics, pattern definition and registration, and random fault densities and distributions; test structures with integral signal processing circuitry; correlations between test structure characteristics and device or circuit properties; and dynamic and reliability test structures.

Package evaluation: methods for measuring device temperature and package heat transfer characteristics; methods for evaluating mechanical integrity; and tests for hermeticity and internal moisture levels.

Testing: models for fault mechanisms; this portion of the effort is expected to link with NBS programs being developed to address broader aspects of testing complex integrated circuit chips and systems.

The goal of the expanded NBS program is to provide the sophisticated metrology, including the underlying knowledge and supporting data, essential for VLSI.

References

1. Bullis, W. M., *Semiconductor Measurement Technology:* Metrology for Submicrometer Devices and Circuits, NBS Spec. Publ. 400-61 (to be published).

2. Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511 (December 1969).

3. Bullis, W. M., Standard Measurements of the Resistivity of Silicon by the Four-Probe Method, NBSIR 74-496 (August 1974).

4. Harman, G. G., and Kessler, H. K., Application of Capacitor Microphones and Magnetic Pickups to the Tuning and Trouble Shooting of Microelectronic Ultrasonic Bonding Equipment, NBS Tech. Note 573 (April 1971).

5. Harman, G. G., Ed., *Semiconductor Measurement Technology:* Microelectronic Ultrasonic Bonding, NBS Spec. Publ. 400-2 (January 1974).

6. Albers, J. H., Ed., *Semiconductor Measurement Technology:* The Destructive Bond Pull Test, NBS Spec. Publ. 400-18 (February 1976).

7. Rubin, S., and Oettinger, F. F., *Semiconductor Measurement Technology:* Thermal Resistance Measurements on Power Transistors, NBS Spec. Publ. 400-14 (April 1979).

8. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F 84, *Annual Book of ASTM Standards,* Part 43 (November 1979).

9. Uriano, G. A., The NBS Standard Reference Materials Program: SRMs Today and Tomorrow, *Standardization News* 7 (9), 8-13 (September 1979).

10. Miller, G. L., Robinson, D. A. H., and Wiley, J. D., Contactless Measurement of Semiconductor Conductivity by Radio Frequency Free-Carrier Power Absorption, *Rev. Sci. Instrum.* 47, 799-805 (1976).

11. Ref. 4, pp. 73-79.

12. Harman, G. G., A Metallurgical Basis for the Non-Destructive Bond Pull-Test, *12th Annual Proceedings, Reliability Physics 1974,* Las Vegas, Nevada, April 2-4, 1974, pp. 205-210.

13. Standard Recommended Practice for Nondestructive Pull Testing of Wire Bonds, ASTM Designation F 458, *Annual Book of ASTM Standards,* Part 43 (November 1979).

14. Standard Methods for Measuring Pull Strength of Microelectronic Wire Bonds, ASTM Designation F 459, *Annual Book of ASTM Standards,* Part 43 (November 1979).

15. Method 2037, Bond Strength, MIL-STD-750B, Test Methods for Semiconductor Devices, Notice 9, 19 September 1978.

16. Method 2011.3, Bond Strength, MIL-STD-883B, Test Methods and Procedures for Microelectronics, Notice 2, 16 May 1979.

17. Harman, G. G., and Cannon, C. A., The Microelectronic Wire Bond Pull Test – How to Use It, How to Abuse It, *IEEE Trans. Components, Hybrids, and Manufacturing Technology* CHMT-1, 203-210 (1978).

18. Thermal Resistance Measurements of Conduction Cooled Power Transistors, EIA Recommended Standard RS-313-B (Revision of RS-313-A) (October 1975).

19. Method 3131.1, Thermal Resistance, MIL-STD-750B, Test Methods for Semiconductor Devices, Notice 9, 19 September 1978.

20. Blackburn, D. L., *Semiconductor Measurement Technology:* Safe Operating Area Limits for Power Transistors – Videotape Script, NBS Spec. Publ. 400-44 (September 1977).

21. Jerke, J. M., Ed., *Semiconductor Measurement Technology:* Accurate Linewidth Measurements on Integrated-Circuit Photomasks, NBS Spec. Publ. 400-43 (February 1980).

22. Nyyssonen, D., Optical Linewidth Measurements on Wafers, *Proc. Soc. Photo-Optical Instrum. Engrs.* 135, *Developments in Semiconductor Microlithography III,* 115-119 (1978).

23. Jerke, J. M., *Semiconductor Measurement Technology:* Optical and Dimensional-Measurement Problems with Photomasking in Microelectronics, NBS Spec. Publ. 400-20 (October 1975).

24. Carver, G. C., Linholm, L. W., and Russell, T. J., The Use of Microelectronic Test Structures to Characterize IC Materials, Processes, and Processing Equipment, *Solid State Technology* (to appear).

25. Schafft, H. A., *Semiconductor Measurement Technology:* ARPA/NBS Workshop III. Test Patterns for Integrated Circuits, NBS Spec. Publ. 400-15 (January 1976).

26. Buehler, M. G., The D-C MOSFET Dopant Profile Method, *J. Electrochem. Soc.* 127, 701-704 (1980).

27. Carver, G. C., and Buehler, M. G., An Analytical Expression for the Evaluation of Leakage Currents in the Integrated Gated-Diode Electrometer (to be published).

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16. ABSTRACT *(A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.)*

The Semiconductor Technology Program at NBS is described briefly; several examples of past successful programs and their significance are given. The work is planned to be expanded significantly beginning in FY 1981. An outline of the present plans for this expansion to cover the problems of very large scale integration (VLSI) is presented.

Note: This material represents four pages of 30 in a chapter covering the role of the U.S. Government in VLSI development. The book is to include 20 other chapters from authors in both industry and universities, and is provisionally titled "Microstructure Science and Technology/VLSI."

17. KEY WORDS *(six to twelve entries; alphabetical order; capitalize only the first letter of the first key word unless a proper name; separated by semicolons)*

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